

Plug-in Signal Conditioners M-UNIT

A/D CONVERTER

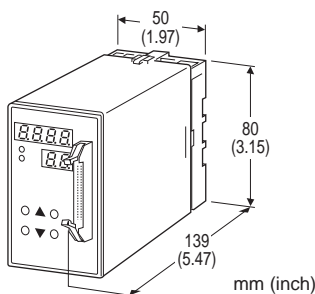
(16-bit resolution)

Functions & Features

- Converts a DC input into parallel digital signals with parity check
- BCD, binary, reflected binary, two's complement outputs selectable
- Open collector or CMOS for output levels
- Output can be scaled and displayed in convenient engineering unit
- Loop test output
- Response time adjustable within 0.15 and 60 sec.

Typical Applications

- Interface of analog signal to computers and PLC
- Input to a digital panel meter



MODEL: AD3V-[1][2]-[3]

ORDERING INFORMATION

• Code number: AD3V-[1][2]-[3]

Specify a code from below for each [1] through [3].
(e.g. AD3V-S1C-M2)

[1] INPUT

Current

Z1: Range 0 - 50 mA DC (Input resistance 100 Ω)

Voltage

S1: Range -1 - +1 V DC (Input resistance 100 kΩ min.)

S2: Range -10 - +10 V DC (Input resistance 1 MΩ min.)

S3: Range -30 - +30 V DC (Input resistance 1 MΩ min.)

[2] OUTPUT LEVEL

A: Open collector

C: CMOS level

[3] POWER INPUT

AC Power

M2: 100 - 240 V AC (Operational voltage range 85 - 264 V, 47 - 66 Hz)

DC Power

R3: 12 - 24 V DC

(Operational voltage range 10.8 - 26.4 V, ripple 10 %p-p max.)

P: 110 V DC

(Operational voltage range 85 - 150 V, ripple 10 %p-p max.)

RELATED PRODUCTS

- Connector terminal block (model: CNT)
- Special cable (model: MCN26)

GENERAL SPECIFICATIONS

Construction: Plug-in

Connection: M3.5 screw terminals and 26-pin connector

Housing material: Flame-resistant resin (black)

Isolation: Input to output to power

Overrange input: Approx. -15 - +115 %

■ DISPLAY

LED: 7 mm (.28") 7 segment, red

Number of display digits: 4 digits for DATA display; 2 digits for ITEM display

PV indication: Output signal in engineering unit

Overrange indication: LEDs blinking

Power saving mode: Displays turn off if the keys are untouched for a preset time period

PL1 (POL) LED: Red light turns on at negative polarity.

PL2 (HOLD) LED: Red light turns on at HOLD.

Setting: (Front key pad)

- Scaled range
- Moving average
- Output code
- Available number of bits
- POL/OVF output logic
- Data output logic
- HOLD input logic
- DAV output logic
- DAV output time
- Output rate 'n' ratio
- Parity check
- etc.

For detailed information, refer to the instruction manual.

INPUT SPECIFICATIONS

■ **DC Current:** 0 - 50 mA DC; shunt resistor attached to input terminals (0.5 W)

Operational range: 0 - 70 mA DC (with 100 Ω/0.5 W)

■ **DC Voltage**

Code S1: -1.00 - +1.00 V DC

Operational range: -1.15 – +1.15 V DC
Code S2: -10.0 – +10.0 V DC
Operational range: -11.5 – +11.5 V DC
Code S3: -30.0 – +30.0 V DC
Operational range: -34.5 – +34.5 V DC
■ **Hold Input:** 5V-CMOS; Negative logic (default)

OUTPUT SPECIFICATIONS

■ **Output Code:** Code and logic are user-selectable.
BCD with polarity
Binary with polarity
Offset binary
Two's complement
Reflected binary
Connector: 26-pin connector (OMRON XG4A-2634)
Paired connector: OMRON XG4M-2630-T, XG5M-263x-N
Cover: OMRON XG5S-2612

■ **Output Level**

- **Open Collector**

Max. collector-emitter voltage: 30 V DC
Max. collector current: 30 mA
Saturation voltage: ≤ 1.1 V
Common: Negative

■ **CMOS Level**

H output: ≥ 4.5 V DC
L output: ≤ 0.5 V DC
Common: Negative

POL output (Polarity): Same logic and level as for the output code; logic user-selectable
OVF output (Overflow): Same logic and level as for the output code; logic user-selectable
DAV output (Data available): Same level as for the output code; logic user-selectable

INSTALLATION

Power consumption

- **AC:** Approx. 10 VA
- **DC:** Approx. 4 W (160 mA at 24 V)

Operating temperature: -5 to +55°C (23 to 131°F)
Operating humidity: 30 to 90 %RH (non-condensing)
Mounting: Surface or DIN rail
Weight: 450 g (0.99 lbs)

PERFORMANCE in percentage of span

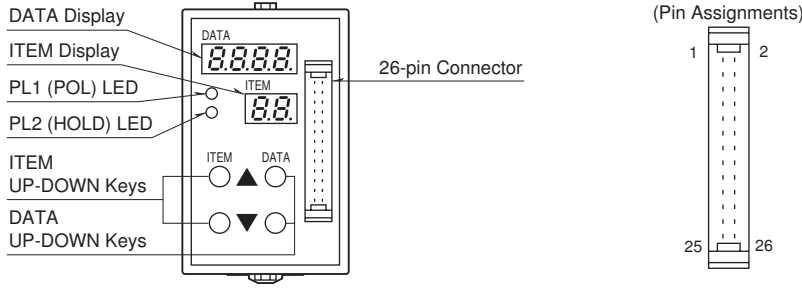
Accuracy: ± 0.1 %
Temp. coefficient: ± 0.015 %/°C (± 0.008 %/°F)
Resolution: 16 bits
Response time: 0.15 – 60 sec. (0 – 90 %) programmable at front key pad.
Line voltage effect: ± 0.1 % over voltage range
Insulation resistance: ≥ 100 M Ω with 500 V DC

Dielectric strength: 2000 V AC @ 1 minute
(input to output to power)
2000 V AC @ 1 minute
(input or output or power to ground)

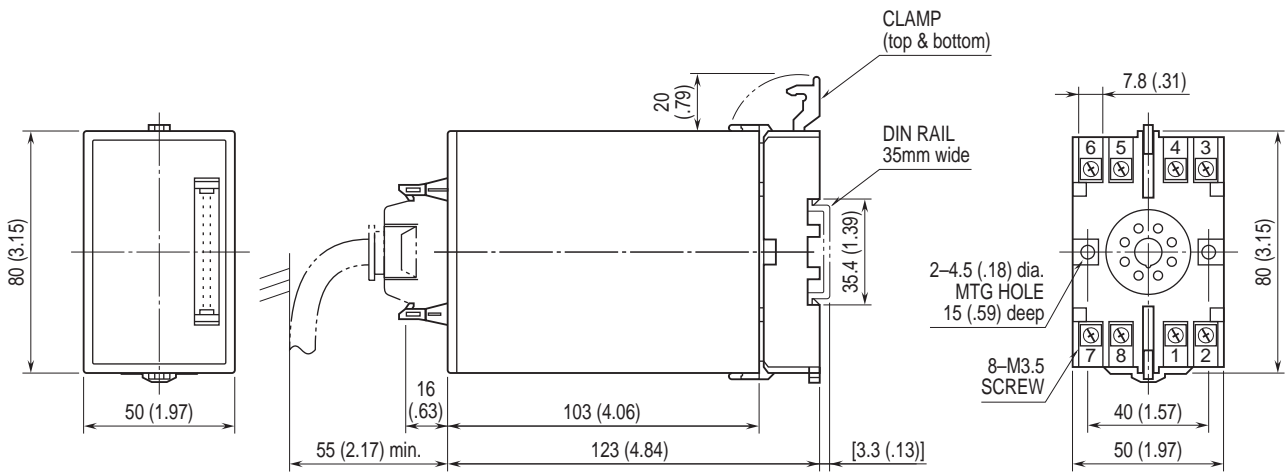
STANDARDS & APPROVALS

CE conformity:
EMC Directive (2004/108/EC)
EMI EN 61000-6-4: 2007
EMS EN 61000-6-2: 2005
Low Voltage Directive (2006/95/EC)
EN 61010-1: 2001
Installation Category II
Pollution Degree 2
Input or output to power: Reinforced insulation (300 V)
Input to output: Basic insulation (300 V)

EXTERNAL VIEW

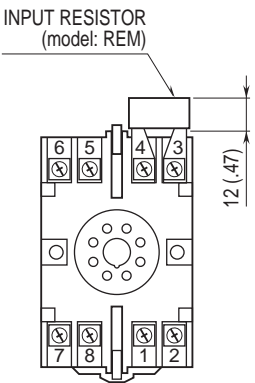


DIMENSIONS unit: mm (inch)



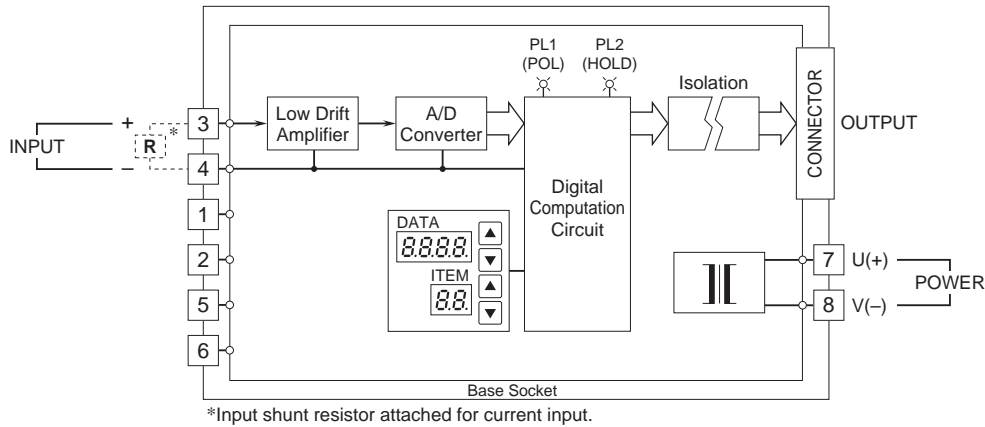
•When mounting, no extra space is needed between units.

TERMINAL ASSIGNMENTS unit: mm (inch)



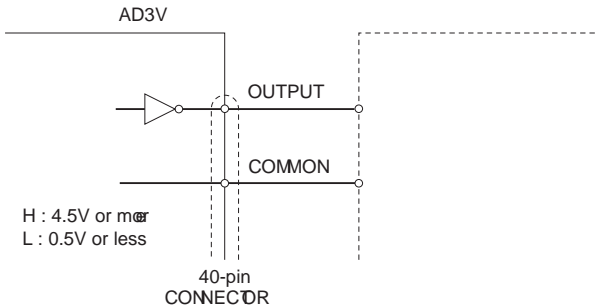
Input shunt resistor attached for current input.

SCHEMATIC CIRCUITRY & CONNECTION DIAGRAM

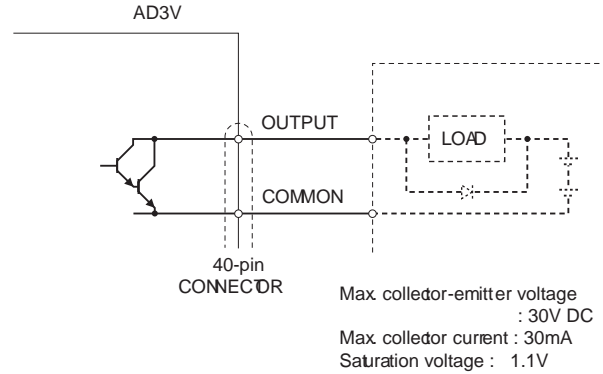


■ Connection Examples

• CMOS LEVEL (5V-CMOS)



• OPEN COLLECTOR



OUTPUT CONNECTOR (26 pins)

• BCD OUTPUT

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	1 10 ⁰	17	COM (-)
2	2 10 ⁰	18	COM (-)
3	4 10 ⁰	19	OVF
4	8 10 ⁰	20	POL
5	1 10 ¹	21	DAV
6	2 10 ¹	22	$\overline{\text{HOLD}}$ *1
7	4 10 ¹	23	P ⁰ *2
8	8 10 ¹	24	P ¹
9	1 10 ²	25	P ²
10	2 10 ²	26	P ³
11	4 10 ²		
12	8 10 ²		
13	1 10 ³		
14	2 10 ³		
15	4 10 ³		
16	8 10 ³		

*1. $\overline{\text{HOLD}}$ signal is for input, the others are for output.

*2. P⁰ corresponds to $\times 10^0$, P¹ to $\times 10^1$, P² to $\times 10^2$, P³ to $n \times 10^3$.

Note: With the number of bits set to 14 (or 12, 10, 8) with ITEM 10, Pin No. 1 – 14 (or 1 – 12, 1 – 10, 1 – 8) are valid.

• BINARY, TWO'S COMPLEMENT OUTPUTS

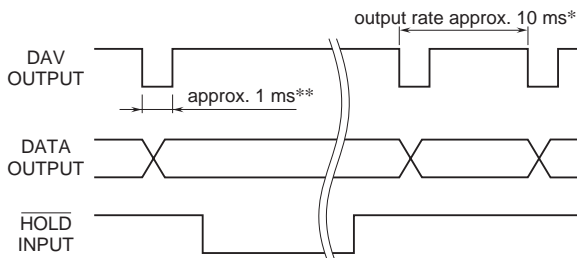
PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	B ⁰	17	COM (-)
2	B ¹	18	COM (-)
3	B ²	19	OVF
4	B ³	20	POL
5	B ⁴	21	DAV
6	B ⁵	22	$\overline{\text{HOLD}}$ *1
7	B ⁶	23	P ⁰ *2
8	B ⁷	24	P ¹
9	B ⁸	25	P ²
10	B ⁹	26	P ³
11	B ¹⁰		
12	B ¹¹		
13	B ¹²		
14	B ¹³		
15	B ¹⁴		
16	B ¹⁵		

*1. $\overline{\text{HOLD}}$ signal is for input, the others are for output.

*2. P⁰ corresponds to B⁰ through B³, P¹ to B⁴ through B⁷, P² to B⁸ through B¹¹, P³ to B¹² through B¹⁵.

Note: With the number of bits set to 14 (or 12, 10, 8) with ITEM 10, Pin No. 1 – 14 (or 1 – 12, 1 – 10, 1 – 8) are valid.

TIMING CHART



Data output is halt during $\overline{\text{HOLD}}$ input.

DAV is output during DATA output.

* Varies by individual module. Set to 'n' times with ITEM 20.

**Selectable with ITEM 17.

INPUT-OUTPUT RELATION EXAMPLES

*FS

-FS stands for -15 % of the input range, which is configured by ITEM22, 0 % input voltage and ITEM23, 100 % input voltage.
 +FS stands for +115 % of the input range.

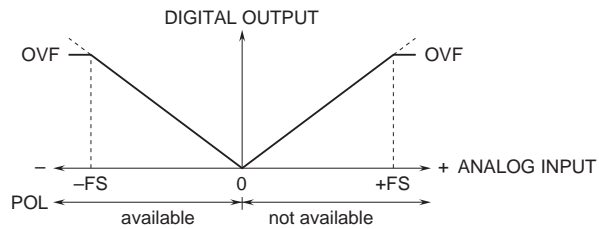
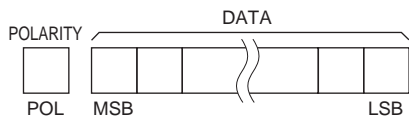
*OVF

When one of the following conditions is true, the digital output overflows (OVF).

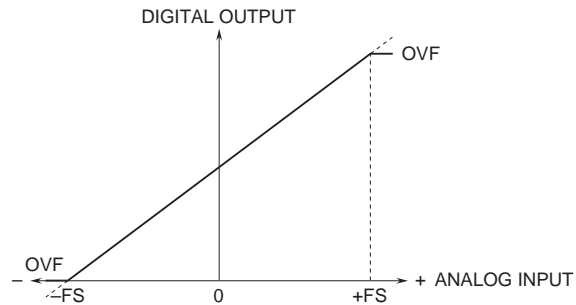
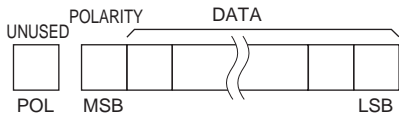
- 1) When the input signal is out of the range between -FS and +FS.
- 2) When the display value (= output signal) exceeds the display range.

The display range differs according to output code. For example, in case of BCD with polarity, it is -9999 to 9999. Please refer to the instruction manual for detail.

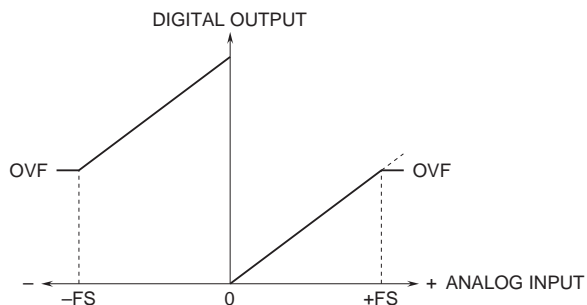
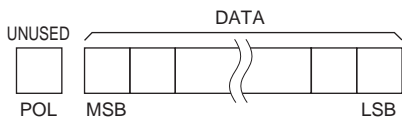
■BCD, BINARY (WITH POLARITY)



■OFFSET BINARY



■TWO'S COMPLEMENT



OUTPUT DATA & PARITY BIT RELATIONSHIP

Hi and Lo indicate the voltage level. Parity logic is unchanged.

■ OPEN COLLECTOR

• Positive Logic I14 : 1, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Lo	Hi
1	Lo	Lo	Lo	Hi	Hi	Lo
2	Lo	Lo	Hi	Lo	Hi	Lo
3	Lo	Lo	Hi	Hi	Lo	Hi
4	Lo	Hi	Lo	Lo	Hi	Lo
5	Lo	Hi	Lo	Hi	Lo	Hi
6	Lo	Hi	Hi	Lo	Lo	Hi
7	Lo	Hi	Hi	Hi	Hi	Lo
8	Hi	Lo	Lo	Lo	Hi	Lo
9	Hi	Lo	Lo	Hi	Lo	Hi
10	Hi	Lo	Hi	Lo	Lo	Hi
11	Hi	Lo	Hi	Hi	Hi	Lo
12	Hi	Hi	Lo	Lo	Lo	Hi
13	Hi	Hi	Lo	Hi	Hi	Lo
14	Hi	Hi	Hi	Lo	Hi	Lo
15	Hi	Hi	Hi	Hi	Lo	Hi

■ CMOS

• Positive Logic I14 : 0, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Hi	Lo
1	Lo	Lo	Lo	Hi	Lo	Hi
2	Lo	Lo	Hi	Lo	Lo	Hi
3	Lo	Lo	Hi	Hi	Hi	Lo
4	Lo	Hi	Lo	Lo	Lo	Hi
5	Lo	Hi	Lo	Hi	Hi	Lo
6	Lo	Hi	Hi	Lo	Hi	Lo
7	Lo	Hi	Hi	Hi	Lo	Hi
8	Hi	Lo	Lo	Lo	Lo	Hi
9	Hi	Lo	Lo	Hi	Hi	Lo
10	Hi	Lo	Hi	Lo	Hi	Lo
11	Hi	Lo	Hi	Hi	Lo	Hi
12	Hi	Hi	Lo	Lo	Hi	Lo
13	Hi	Hi	Lo	Hi	Lo	Hi
14	Hi	Hi	Hi	Lo	Lo	Hi
15	Hi	Hi	Hi	Hi	Hi	Lo

• Negative Logic I14 : 0, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Lo	Hi
1	Hi	Hi	Hi	Lo	Hi	Lo
2	Hi	Hi	Lo	Hi	Hi	Lo
3	Hi	Hi	Lo	Lo	Lo	Hi
4	Hi	Lo	Hi	Hi	Hi	Lo
5	Hi	Lo	Hi	Lo	Lo	Hi
6	Hi	Lo	Lo	Hi	Lo	Hi
7	Hi	Lo	Lo	Lo	Hi	Lo
8	Lo	Hi	Hi	Hi	Hi	Lo
9	Lo	Hi	Hi	Lo	Lo	Hi
10	Lo	Hi	Lo	Hi	Lo	Hi
11	Lo	Hi	Lo	Lo	Hi	Lo
12	Lo	Lo	Hi	Hi	Lo	Hi
13	Lo	Lo	Hi	Lo	Hi	Lo
14	Lo	Lo	Lo	Hi	Hi	Lo
15	Lo	Lo	Lo	Lo	Lo	Hi

• Negative Logic I14 : 1, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Hi	Lo
1	Hi	Hi	Hi	Lo	Lo	Hi
2	Hi	Hi	Lo	Hi	Lo	Hi
3	Hi	Hi	Lo	Lo	Hi	Lo
4	Hi	Lo	Hi	Hi	Lo	Hi
5	Hi	Lo	Hi	Lo	Hi	Lo
6	Hi	Lo	Lo	Hi	Hi	Lo
7	Hi	Lo	Lo	Lo	Lo	Hi
8	Lo	Hi	Hi	Hi	Lo	Hi
9	Lo	Hi	Hi	Lo	Hi	Lo
10	Lo	Hi	Lo	Hi	Hi	Lo
11	Lo	Hi	Lo	Lo	Lo	Hi
12	Lo	Lo	Hi	Hi	Hi	Lo
13	Lo	Lo	Hi	Lo	Lo	Hi
14	Lo	Lo	Lo	Hi	Lo	Hi
15	Lo	Lo	Lo	Lo	Hi	Lo



Specifications are subject to change without notice.